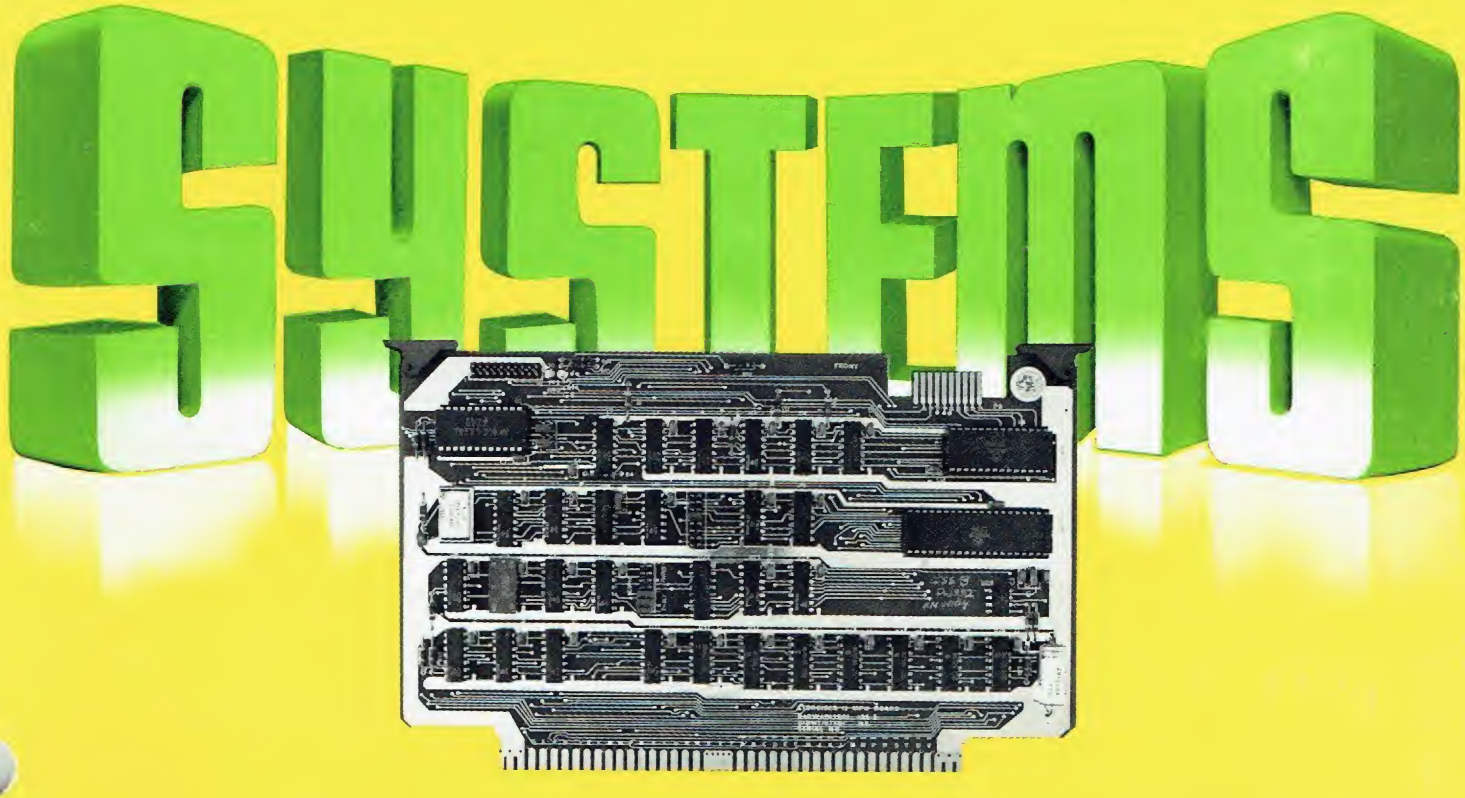
MOTOROLA

MEX68B00(D)

MEX6800-2
MPU II MODULE

User's Guide



MICROSYSTEMS

MEX68B00(D)
JUNE 1978

MEX6800-2

MPU II MODULE
USER'S GUIDE

First Edition

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CHAPTER 1

GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides general information, installation instructions, programming considerations, and theory of operation for the MEX6800-2 MPU II Module. A typical module is shown in Figure 1-1. All address references within this manual are shown in hexadecimal unless otherwise indicated.

1.2 FEATURES

The features of the MPU II Module include:

- MC68B00 Microprocessing Unit (MPU) with associated clock oscillator, and power on restart timer.
- MPU is 8 bit parallel device capable of addressing 64K bytes of memory.
- Responds to real time interrupts.
- Selectable memory speed of 1.0, 1.5, or 2.0 MHz on module. (Jumper selectable external clock capability.
- Series II DSB (Dynamic System Bus) for Priority Interrupt Control MC6828.
- Bus drive capability.
- TTL signal level inputs and TTL signal level, three-state, or open collector outputs.

1.3 SPECIFICATIONS

The MPU II Module specifications are identified in Table 1-1.

1.4 GENERAL DESCRIPTION

The MPU II Module serves a double function in the system. This module provides the timing and microprocessing unit for both the Motorola system and the user's prototype system. The timing circuit on the module determines the system frequency and provides the system with the capability to refresh dynamic memories. The module also interfaces the MC68B00 Microprocessing Unit (MPU) with the system bus. The MPU performs all of the EXbug Firmware and user's program instructions.

This module could also serve as an MPU module for any system built around the MC68B00. The signal $\overline{\text{EXBUG}}$, when high, makes the MPU a completely independent module.

In the upper left-hand portion of the module is a 20-pin header, P2, known as the Dynamic System Bus (DSB). Interrupt inputs for the MC6828 Priority Interrupt Controller (PIC) from external peripheral modules may be connected through the DSB.

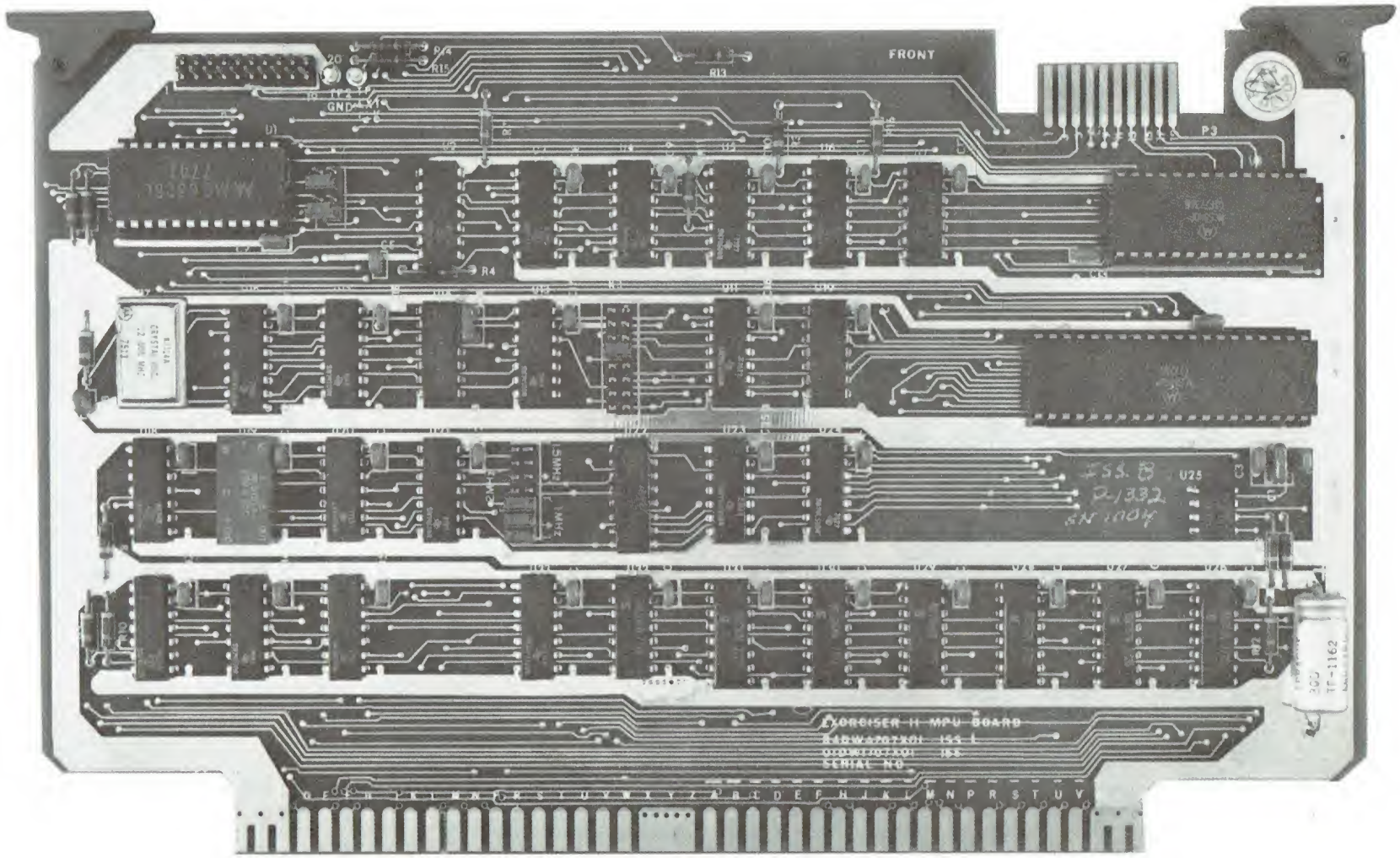


FIGURE 1-1. MPU II Module

Jumper selectable internal or external clock is provided on the module. The internal clock provides three, jumper selectable, speeds for memory (1.0, 1.5, or 2.0 MHz).

Hardware external to the MPU II Module may make use of the Programmable Timer Module (PTM) MC6840 (a plug-in device) which is circuitry connected to edge connector P3. The decoding for the PTM is jumper selectable on the MPU II Module.

TABLE 1-1. MPU II Module Specifications

CHARACTERISTIC	SPECIFICATION
Microprocessor	MC68B00 MPU
Word Size	
Data	8 bits
Address	16 bits
Instructions	8, 16, or 24 bits
Instructions	72 variable length instructions
Addressing Modes	Seven Addressing Modes: Direct, Relative, Immediate, Indexed, Extended, Implied, and Accumulator.
Clock Signal	Crystal controlled 12 MHz with logic for generating 2 phase non-overlapping signal to MPU and system bus.
Memory Speed	Internal or external jumper selectable. Internal jumper selectable 1.0, 1.5, or 2.0 MHz speed.
Address Capability	65K bytes
Interrupts	
External	$\overline{IRQ}$ maskable interrupt and $\overline{NMI}$ non-maskable interrupt.
Input Signals	
Commands	TTL voltage compatible
Address	TTL voltage compatible
Data Bus	Three-state TTL voltage compatible
Operating Temperature	0^{o} to 70^{o} C
Power Requirements	+5 Vdc at 2.0 A (max)
Dimensions	
Width x Height	9.75 in. x 6.15 in.
Board Thickness	0.062 in.

CHAPTER 2

INSTALLATION INSTRUCTIONS, PROGRAMMING AND INTERCONNECTION CONSIDERATIONS

2.1 INTRODUCTION

This chapter provides the unpacking, inspection, installation, programming, and interconnection instructions for the MPU II Module. This chapter also discusses the Module's interconnection signals and the programming considerations.

2.2 UNPACKING INSTRUCTIONS

Unpack the MPU II Module from its shipping carton and, referring to the packing list, verify that all the items are present. Save the packing material for storing and shipping the module. If the shipping carton is damaged upon receipt, request that the carrier's agent be present while the module is being unpacked and inspected.

2.3 INSPECTION

The MPU II Module should be inspected upon receipt for broken, damaged or missing parts, and physical damage to the printed circuit board.

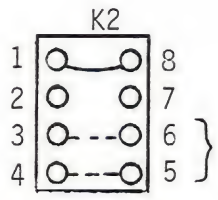
2.4 HARDWARE PREPARATION

Figure 2-1 illustrates the location of the user options that are available on the MPU II Module. The user must decide at what clock speed the system will operate, and whether the Programmable Timer Module (PTM) and/or the Priority Interrupt Controller (PIC) are required for 1 MHz applications.

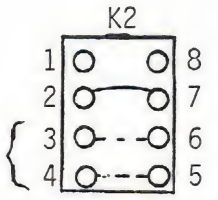
2.4.1 System Speed Selection

The user has the choice of using the MPU II Module as the system clock or, through a jumper, connecting to an external clock.

Depending upon the system configuration and the development requirements of the target system, the user must select either the internal or external clock option. When selecting internal clock, the user has a choice of fixed clock rates of 1.0, 1.5, or 2.0 MHz. An external clock may be connected to provide a continuous range of speeds below 2.0 MHz. The top half of jumper K2 is used to select internal or external clock. A plug-in jumper is provided.



EXTERNAL CLOCK



INTERNAL CLOCK

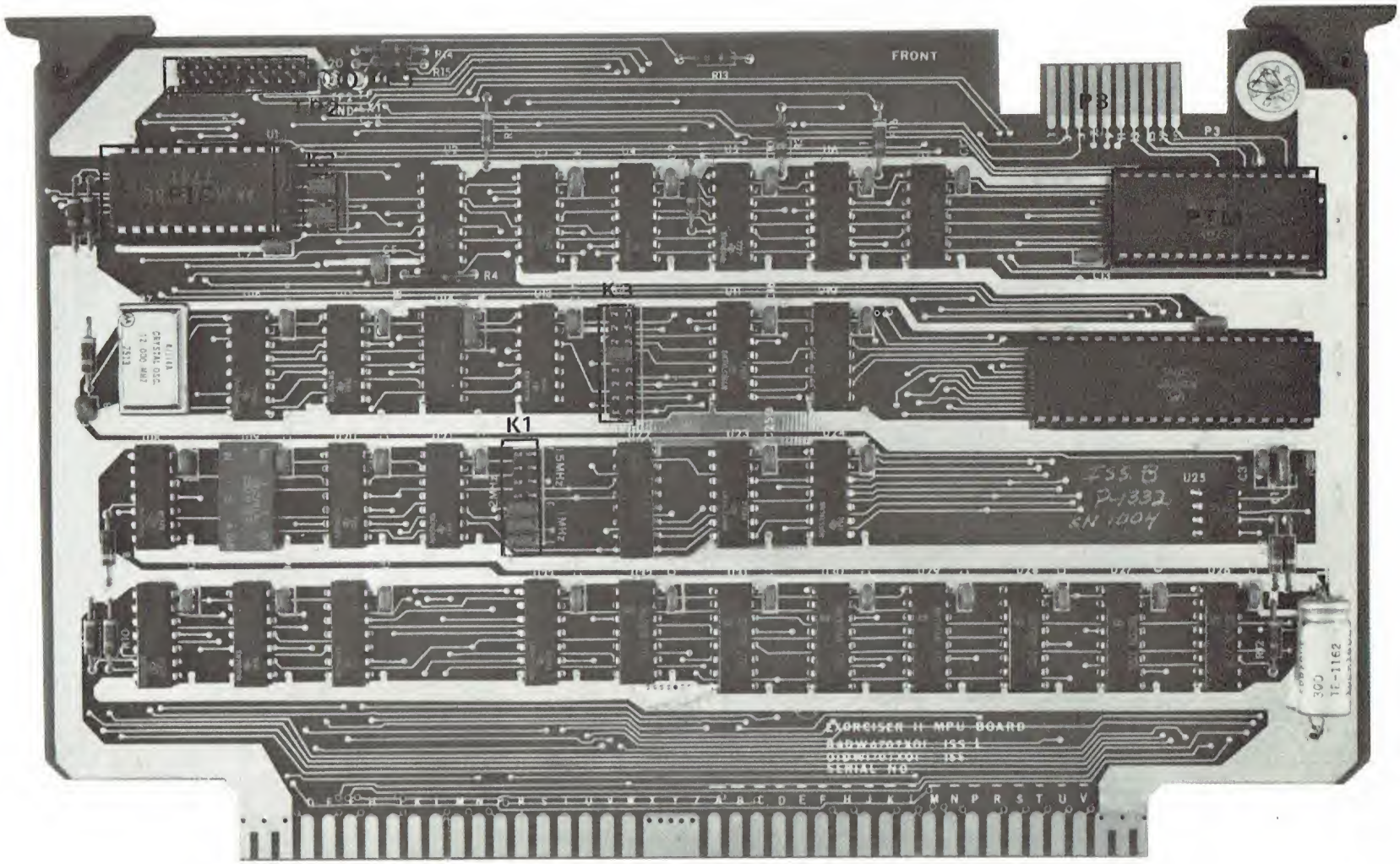
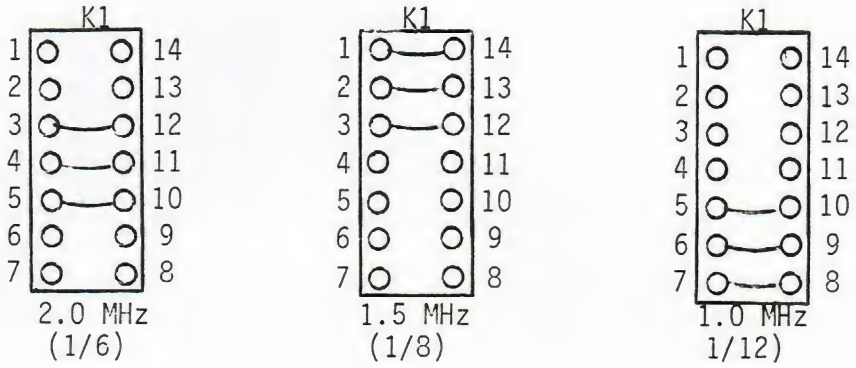


FIGURE 2-1. MPU II Module User Option Locations

When external clock is selected, the user should connect the clock input to TP1 (see Figure 2-1). The TP2 may be used as a convenient ground for this input. The input signal must be TTL compatible and is fed through divider logic that produces the actual processor clock. The three options described below allow the board frequency to be 1/12, 1/8, or 1/6 of the external clock source. One of the three options must be made to properly operate the system.

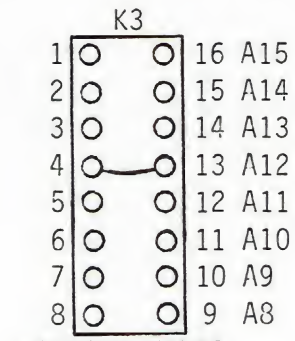
When internal clock is selected, the clock source to the divider logic is fixed at 12.0 MHz to yield 2.0, 1.5, and 1.0 MHz for each of the following jumper configurations. Jumper K1 is used to select one of the three speed ranges. Plug-in jumpers are provided.

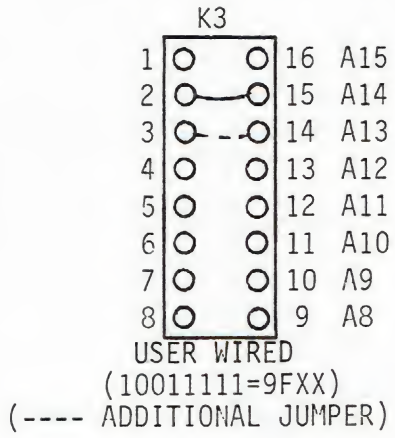


2.4.2 Programmable Timer Option

The Programmable Timer Module (PTM) MC6840 may be used when an internal timer function is desired. Due to speed limitations of the MC6840, the option may be used only when the MPU II Module is configured for 1 MHz operation.

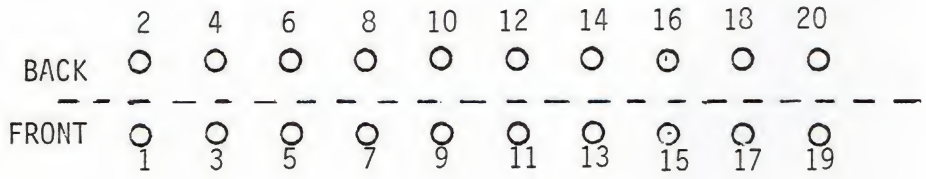
The standard addressing of this device is set at the factory to occupy locations $EF00-EF07. Due to incomplete decoding of the address lines, the entire block ($EF00-EFFF) responds to the above set of addresses. The user has the option of changing the decoding of the upper (most significant) eight bits of the address for the timer. Jumper K3 is provided for this purpose. An installed jumper represents a binary ZERO, and an uninstalled jumper represents a binary ONE. A plug-in jumper is provided.





Additional jumpers may be added to change the decoding.

Hardware external to the MPU II Module may make use of the PTM when connected to edge connector P3 (see Figure 2-1). Asynchronous input/output are circuitry connected to P3, as shown below.



PIN	SIGNAL
1	NOT USED
3	TIMER OUTPUT O1
5	TIMER OUTPUT O2
7	TIMER OUTPUT O3
9	$\overline{\text{GATE}}$ INPUT $\overline{\text{G1}}$
11	$\overline{\text{CLOCK}}$ INPUT $\overline{\text{C1}}$
13	$\overline{\text{CLOCK}}$ INPUT $\overline{\text{C3}}$
15	$\overline{\text{GATE}}$ INPUT $\overline{\text{G3}}$
17	$\overline{\text{CLOCK}}$ INPUT $\overline{\text{C2}}$
19	$\overline{\text{GATE}}$ INPUT $\overline{\text{G2}}$
2 thru 20	GND

Connector P3, pins 11, 13, and 17 will accept asynchronous TTL voltage level signals to decrement Timers 1, 2, and 3, respectively.

Connector P3, pins 9, 15, and 19 will accept asynchronous TTL compatible signals which are used as triggers or clock gating functions to Timers 1, 2, and 3, respectively.

Connector P3, pins 3, 5, and 7, Timer outputs O1, O2, and O3 are capable of driving up to two TTL loads and produce a defined output waveform for either Continuous or Single-shot Timer modes.

Refer to MC6840 Data Sheet for detailed information on the Programmable Timer Module.

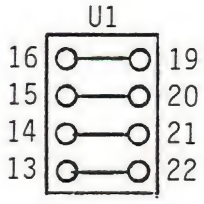
2.4.3 Priority Interrupt Controller

If the user requires a priority interrupt facility, the Priority Interrupt Controller (PIC) MC6828 may be plugged into location U1. This option may only be used when the MPU II Module is configured for 1.0 MHz or slower operation.

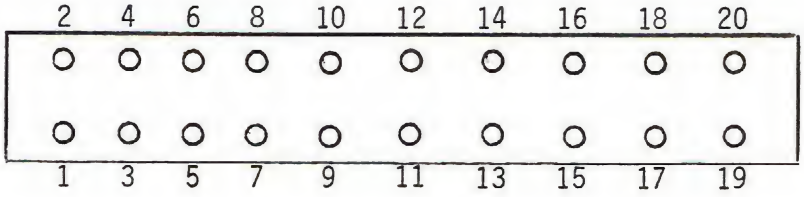
NOTE

The MC6828 should be removed and replaced with the jumper platform provided for operating speeds greater than 1.0 MHz.

The jumper platform supplied provides the following connections to the U1 socket.



Inputs to the PIC may be connected through the Dynamic System Bus (DSB) P2 (see Figure 2-1). The DSB is organized as shown below:



PIN	SIGNAL
1	GND
2	$\overline{\text{INTERRUPT 0}}$
3	$\overline{\text{INTERRUPT 1}}$
4	$\overline{\text{INTERRUPT 2}}$
5	$\overline{\text{INTERRUPT 3}}$
6	$\overline{\text{INTERRUPT 4}}$
7	$\overline{\text{INTERRUPT 5}}$
8	$\overline{\text{INTERRUPT 6}}$
9	$\overline{\text{INTERRUPT 7}}$
10 thru 17	NOT USED
18	GND
19	NOT USED
20	GND

2.5 PIC PROGRAMMING INFORMATION

The PIC is used to add prioritized responses to inputs in the system. MC6828 modifies the vector address which the processor uses to find the start of the polling or other interrupt service routine. Each interrupting device is assigned a unique ROM location which contains the starting address of the appropriate service routine. After the MPU detects and responds to an interrupt, the PIC directs the MPU to the proper memory location.

If the user is using more than one peripheral device capable of interrupting the MPU, a software interrupt polling routine must be prepared to interrogate each of these devices and determine the device initiating the interrupt. This polling routine, on determining the $\overline{\text{IRQ}}$ initiated device, causes the MPU to vector the appropriate service routine.

In preparing the interrogation routine, priorities must be assigned to the devices by assigning their position in the interrogation polling routine. The device interrogated first has the highest priority, and the device interrogated last has the lowest priority.

2.6 INSTALLATION INSTRUCTIONS

Install the MPU II Module as follows:

a. Turn equipment power OFF.

CAUTION

INSERTING AN MPU II MODULE WHILE POWER IS APPLIED MAY RESULT IN DAMAGE TO COMPONENTS ON THE MODULE.

b. Install the module in the selected card slot.

c. Connect any cable to P3 (if used) and any wiring to P2 and TP1 or TP2 (if used).

d. Turn equipment power ON.

2.7 MODULE INTERCONNECTIONS

The MPU II Module interconnects directly with the system bus. The bus signals are identified in Table 2-1. Table 2-2 identifies the Dynamic System Bus Interface signals on connector P2. Table 2-3 identifies the Timer Interface signals on connector P3.

TABLE 2-1. Connector P1 Bus Interface Signals

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
A,B,C	+5V	+5 Vdc - Used by the module logic circuits
D	$\overline{IRQ}$	INTERRUPT REQUEST - A low level sensitive input signal to the MPU II Module used to request generation of an MPU interrupt sequence. The MPU will wait until it completes the instruction being executed before it recognizes the request. At that time, if the interrupt mask bit in the MPU Condition Code Register is not set, the MPU will begin executing the interrupt sequence.
E	$\overline{NMI}$	NON-MASKABLE INTERRUPT - A low going, edge sensitive input signal to the MPU II Module used to request generation of an MPU non-maskable interrupt sequence. The MPU will wait until it completes the instruction being executed before it recognizes the request. At that time, regardless of the logic state of the Interrupt Mask bit in the MPU Condition Code Register, the MPU will begin executing the non-maskable interrupt.

TABLE 2-1. Connector P1 Bus Interface Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
F	VMA	VALID MEMORY ADDRESS - A high level, TTL compatible signal produced by the MPU II Module and used to indicate to the DEbug II Module that a valid memory address is present on the address bus.
H	---	NOT USED - Reserved for system expansion.
J	Ø2	Phase 2 - One of the bi-phase clock signals generated by the clock circuit on the MPU II Module.
K		Not Used
L	MEM CLK	MEMORY CLOCK - An ungated, TTL level Ø2 clock signal used to refresh all dynamic Random Access Memory modules within the system.
M		Not Used
N	$\overline{TSC}$	THREE-STATE CONTROL - This input signal to the MPU II Module, when low, places all of the address and data lines on the module into their off or high impedance state. The tri-stated and BA signals will also be forced low. Since the MPU is a dynamic device, it should not be held in the THREE-STATE CONTROL mode for more than 9.5 microseconds.
P	BA	BUS AVAILABLE - A normally low level output signal from the MPU II Module that, when activated, goes high to indicate that the MPU has halted and the address bus is available. This condition occurs whenever the GO/HALT signal is in the HALT (low) state or the MPU is in the WAIT state as a result of executing a Wait instruction. When this occurs, all of the MPU three-state output drivers will go to their off (high impedance) state and other outputs to their normally inactive state. A maskable interrupt or non-maskable interrupt removes the MPU from the WAIT state.
R	$\overline{MEM\ RDY}$	MEMORY READY - A signal generated by the user that permits the system to work with slow memory modules. When this signal is at a low level, the Ø1 and Ø2 clock signals are stretched, with the O1 signal held low and the Ø2 signal held high for a period of one clock cycle.
S,T,U V,W		Not Used
X,Y,Z	GND	GROUND

TABLE 2-1. Connector P1 Bus Interface Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
$\overline{A}$ - $\overline{F}$		Not Used
$\overline{H}$	$\overline{D3}$	DATA bus (bit 3) - One of 8 bi-directional data lines used to provide a two-way data transfer between the MPU II Module and all other plug-in modules within the system. The data bus drivers on the other modules are in their off or high impedance state except when selected during a memory read or write operation.
$\overline{J}$	$\overline{D7}$	DATA bus (bit 7) - Same as $\overline{D3}$ on Pin $\overline{H}$.
$\overline{K}$	$\overline{D2}$	DATA bus (bit 2) - Same as $\overline{D3}$ on Pin $\overline{H}$.
$\overline{L}$	$\overline{D6}$	DATA bus (bit 6) - Same as $\overline{D3}$ on Pin $\overline{H}$.
$\overline{M}$	A14	ADDRESS bus (bit 14) - One of 16 address lines from the MPU II Module that permits the MPU to select any addressable memory location within the system.
$\overline{N}$	A13	ADDRESS bus (bit 13) - Same as A14 on Pin $\overline{M}$.
$\overline{P}$	A10	ADDRESS bus (bit 10) - Same as A14 on Pin $\overline{M}$.
$\overline{R}$	A9	ADDRESS bus (bit 9) - Same as A14 on Pin $\overline{M}$.
$\overline{S}$	A6	ADDRESS bus (bit 6) - Same as A14 on Pin $\overline{M}$.
$\overline{T}$	A5	ADDRESS bus (bit 5) - Same as A14 on Pin $\overline{M}$.
$\overline{U}$	A2	ADDRESS bus (bit 2) - Same as A14 on Pin $\overline{M}$.
$\overline{V}$	A1	ADDRESS bus (bit 1) - Same as A14 on Pin $\overline{M}$.
$\overline{W}$,$\overline{X}$,$\overline{Y}$	GND	GROUND
1,2,3	+5V	+5 Vdc - Used by the module logic circuits.
4	G/H	GO/HALT - When this input to the MPU II Module is in the high state, the MPU will fetch the instruction addressed by the program counter and start instruction execution. When low, all activity in the MPU will be halted. This input is level sensitive. In the HALT mode, the MPU will stop at the end of an instruction, the BUS AVAILABLE signal will go high, the VALID MEMORY ADDRESS signal will be tri-state, and all other three-state lines will be changed to their off or high impedance state.

TABLE 2-1. Connector P1 Bus Interface Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
5	$\overline{\text{RESET}}$	RESET - This input signal to the MPU Module is used to restart the system when power is initially applied. Restart occurs on the low-to-high transition of the RESTART signal. If the RESTART pushbutton switch, located on the front panel of the system, is depressed while the system is operating, the low-to-high transition of the RESET signal will cause the MPU II Module to execute the EXbug restart routine or the restart routine indicated by the user.
6	R/W	READ/WRITE - This signal is generated by the MPU II Module, and indicates to the other modules contained within the system that the MPU is performing a memory read (high) or write (low) operation. The normal standby state of this signal is read (high). Additionally, when the MPU is halted, this signal will be in the read state.
7	Ø1	Phase 1 - One of the bi-phase clock signals generated by the clock circuit on the MPU II Module.
8,9		Not Used
10	VUA	VALID USER'S ADDRESS - This signal is produced by the DEbug II Module. When high, this signal indicates that the address on the address bus is valid and the MPU II Module is NOT addressing the EXbug Program.
11		Not Used
12	$\overline{\text{REF REQ}}$	REFRESH REQUEST - This input signal to the MPU II Module, when low, initiates a memory refresh cycle of the dynamic memory modules. During the refresh operation, the clock is inhibited from generating its Ø1 (held high) and Ø2 (held low) clock signals. However, during a refresh operation, the MEM CLK signal is still generated in order to provide the necessary refresh clock.
13	REF GRANT	REFRESH GRANT - This output signal from the MPU II Module, when high, instructs the dynamic memory modules to refresh their memories.
14	$\overline{\text{DEBUG}}$	DEBUG - This low level signal from the DEbug II Module indicates to the MPU II Module that the DEbug II Module is installed in the system. This is used to determine whether the VALID USER'S ADDRESS (VUA) signal is controlled by the DEbug II Module or the MPU II Module. When the DEbug II Module is NOT used, the MPU II Module forces this signal line high.
16,17		Not Used

TABLE 2-1. Connector P1 Bus Interface Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
18	CLOCK	CLOCK - A free running, symmetrical clock signal generated on the MPU Module, and available to peripheral modules that require a clock not affected by MPU and/or memory timings. This clock signal has the same frequency as MEM CLK, but is not stretched during slow memory operations (initiated by the MEM RDY signal on Pin R).
19		Not Used
20,21,22	GND	GROUND
23 - 28		Not Used
29	$\overline{D1}$	DATA bus (bit 1) - Same as $\overline{D3}$ on Pin $\overline{H}$.
30	$\overline{D5}$	DATA bus (bit 5) - Same as $\overline{D3}$ on Pin $\overline{H}$.
31	$\overline{D\emptyset}$	DATA bus (bit Ø) - Same as $\overline{D3}$ on Pin $\overline{H}$.
32	$\overline{D4}$	DATA bus (bit 4) - Same as $\overline{D3}$ on Pin $\overline{H}$.
33	A15	ADDRESS bus (bit 15) - Same as A14 on Pin $\overline{M}$.
34	A12	ADDRESS bus (bit 12) - Same as A14 on Pin $\overline{M}$.
35	A11	ADDRESS bus (bit 11) - Same as A14 on Pin $\overline{M}$.
36	A8	ADDRESS bus (bit 8) - Same as A14 on Pin $\overline{M}$.
37	A7	ADDRESS bus (bit 7) - Same as A14 on Pin $\overline{M}$.
38	A4	ADDRESS bus (bit 4) - Same as A14 on Pin $\overline{M}$.
39	A3	ADDRESS bus (bit 3) - Same as A14 on Pin $\overline{M}$.
40	AØ	ADDRESS bus (bit Ø) - Same as A14 on Pin $\overline{M}$.
41,42,43	GND	ground

TABLE 2-2. Connector P2 Dynamic System Bus

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
1	GND	GROUND
2	$\overline{IN0}$	INTERRUPT 0 - Low level input to PIC for prioritized responses to MPU.
3	$\overline{IN1}$	INTERRUPT 1 - Same as P2-2
4	$\overline{IN2}$	INTERRUPT 2 - Same as P2-2
5	$\overline{IN3}$	INTERRUPT 3 - Same as P2-2
6	$\overline{IN4}$	INTERRUPT 4 - Same as P2-2
7	$\overline{IN5}$	INTERRUPT 5 - Same as P2-2
8	$\overline{IN6}$	INTERRUPT 6 - Same as P 2-2
9	$\overline{IN7}$	INTERRUPT 7 - Same as P2-2
11 - 17		Not Used
18	GND	GROUND
19		Not Used
20	GND	GROUND

TABLE 2-3. Connector P3 Timer Interface Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1		Not Used
3	O1	TIMER OUTPUT O1 - High level output from PTM capable of driving up to two TTL loads.
5	O1	TIMER OUTPUT O2 - Same as P3-3.
7	O3	TIMER OUTPUT O3 - Same as P3-3.
9	$\overline{G1}$	GATE INPUT 1 - Low level asynchronous TTL compatible input signal as trigger or clock gating to Timer.
11	$\overline{C1}$	CLOCK INPUT 1 - Low level asynchronous TTL voltage level input signal used to decrement Timer.
13	$\overline{C3}$	CLOCK INPUT 3 - Same as P3-11.
15	$\overline{G3}$	GATE INPUT 3 - Same as P3-9.
17	$\overline{C2}$	CLOCK INPUT 2 - Same as P3-11.
19	$\overline{G2}$	GATE INPUT 2 - Same as P3-9.
2,4,6,8, 10,12,14, 16,18,20	GND	GROUND

CHAPTER 3

THEORY OF OPERATION

3.1 INTRODUCTION

This chapter provides a block diagram description of the MEX6800-2 MPU II Module. A block diagram of this module is illustrated in Figure 3-1, and the schematic diagram in Figure 3-2.

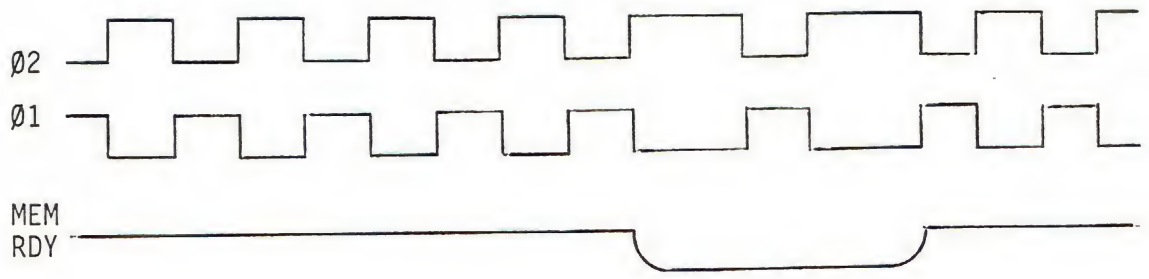
3.2 DESCRIPTION

The MPU II Module, as illustrated in Figure 3-1, provides the user with the option of using its internal clock (1.0, 1.5, 2.0 MHz) or an external clock signal. The MPU II Module is capable of accepting an external clock input between 600 KHz and 12.0 MHz, and off that frequency (Xo), it is capable of generating three basic frequencies: Xo/6, Xo/8, Xo/12. This basic frequency should be within the M68B00 specification, 100 KHz $\leq$ Xo/6, Xo/8, Xo/12 $\leq$ 2.0 MHz. The output selected is determined by the position of K1. The external clock signal is applied to the EXT CLK input terminals. Jumper K2 determines which of the two clock sources (external, internal) is applied to the clock.

The clock control circuit converts its selected input clock signal into two non-overlapping clock signals, Ø1 and Ø2, required by the M68B00 Microprocessing Unit and the system. This clock control circuit also applies the Ø2 clock to the Priority Interrupt Controller (PIC) and, with the R/W signal, it is applied to the data bus control circuit. DBE (Data Bus Enable) is another clock generated by the clock control circuitry. This signal enables the system to transfer data on its bus during a write cycle.

The clock control circuit also provides the MPU II Module with MEM CLK signal required for dynamic memory operation. For the dynamic memory operation, the clock control circuit provides the dynamic memory refresh capability as soon as a REFRESH REQUEST ($\overline{\text{REF REQ}}$) signal is detected on the system's bus. The clock control circuit also provides the MPU II Module with a dynamic memory refresh capability. Any dynamic memory module in the system can initiate a memory refresh operation by placing a $\overline{\text{RR}}$ (Refresh Request) command on the system bus. Assume that a dynamic memory module has just applied a $\overline{\text{RR}}$ command to the timing control circuit. This $\overline{\text{RR}}$ command inhibits the timing control from generating its Ø1 and Ø2 clock signals with Ø1 present and, at the same time, instructs the timing control circuit to generate a RG (Refresh Grant or REF GRANT) command. The RG command instructs the requesting memory to refresh itself using the MEM CLK, and remove the $\overline{\text{RR}}$ command. The memory control, on the removal of the $\overline{\text{RR}}$ command, is again enabled to generate Ø1 and Ø2 clock.

The MPU II Module, through the $\overline{\text{MEMORY READY}}$ command, has the capability of working with slow memory modules. The $\overline{\text{MEMORY READY}}$ command, on going low, will cause a stretch of the cycle while Ø2 is kept high and Ø1 is kept low for extra cycle, as shown below.



The Three-State Control Circuit, on receiving a low level $\overline{TSC}$ (Tri-State Control), will generate TSG (Tri-State Grant) and simultaneously will hold Ø1 and Ø2 to MPU in the High, Low state, respectively, while the clock signals to the bus operate in their regular modes of operation. Since the MPU 68B00 is a dynamic device, Ø1 and Ø2 should not be kept in one state for more than 9500 microseconds. TSG signal also drives the data bus, address bus, R/W signal (VMA, VUA in the DEbug Module is not in the system) to their off or high impedance state -- that is, these drivers place a high impedance output to the system bus.

Another approach to DMA (Direct Memory Access) operation is through the use of $\overline{G/H}$. When this signal is driven by the user to its low state, the MPU will respond with BA (Bus Available) signal after termination of the execution of current instructions, indicating that the bus is available for user's use. Under this mode, the data bus, address bus, and R/W lines will go to their off or high impedance state. VMA, VUA signals will go to their off state in this mode, if the DEbug II Module is not in the system. When DEbug II Module is in the system, these two signal states will be handled by this module.

The R/W control circuitry determines the transfer of data into or out of the MC68B00 Microprocessing Unit.

The restart circuit generates a $\overline{RESET}$ signal approximately 500 ms after power is applied to the module. This module also receives a $\overline{RESET}$ signal each time the system RESTART switch is activated. The $\overline{RESET}$ signal instructs the MC68B00 Microprocessing Unit to perform its initialization routine. This signal also initializes the Programmable Timer (MC6840).

The Programmable Timer (MC6840) is a programmable subsystem component of the MC6800 family designed to provide variable system time intervals. This device actually occupies only eight memory locations ($EF00-EF07) and the rest of the block is occupied by the device due to the address decoding scheme. The user has the capability of decoding the two most significant bits of the four-bit address. This is done on Timer ADDRESS select (K3).

The Priority Interrupt Controller (PIC) (MC6828) is used to add prioritized responses to inputs in the system. The MC6828 modifies the vector address which the processor uses to find the start of the polling or other interrupt serving routine. With the PIC, each interrupting device is assigned a unique ROM location which contains the starting address of the appropriate service routine. After the MPU detects and responds to an interrupt, the PIC directs the MPU to the proper memory location.

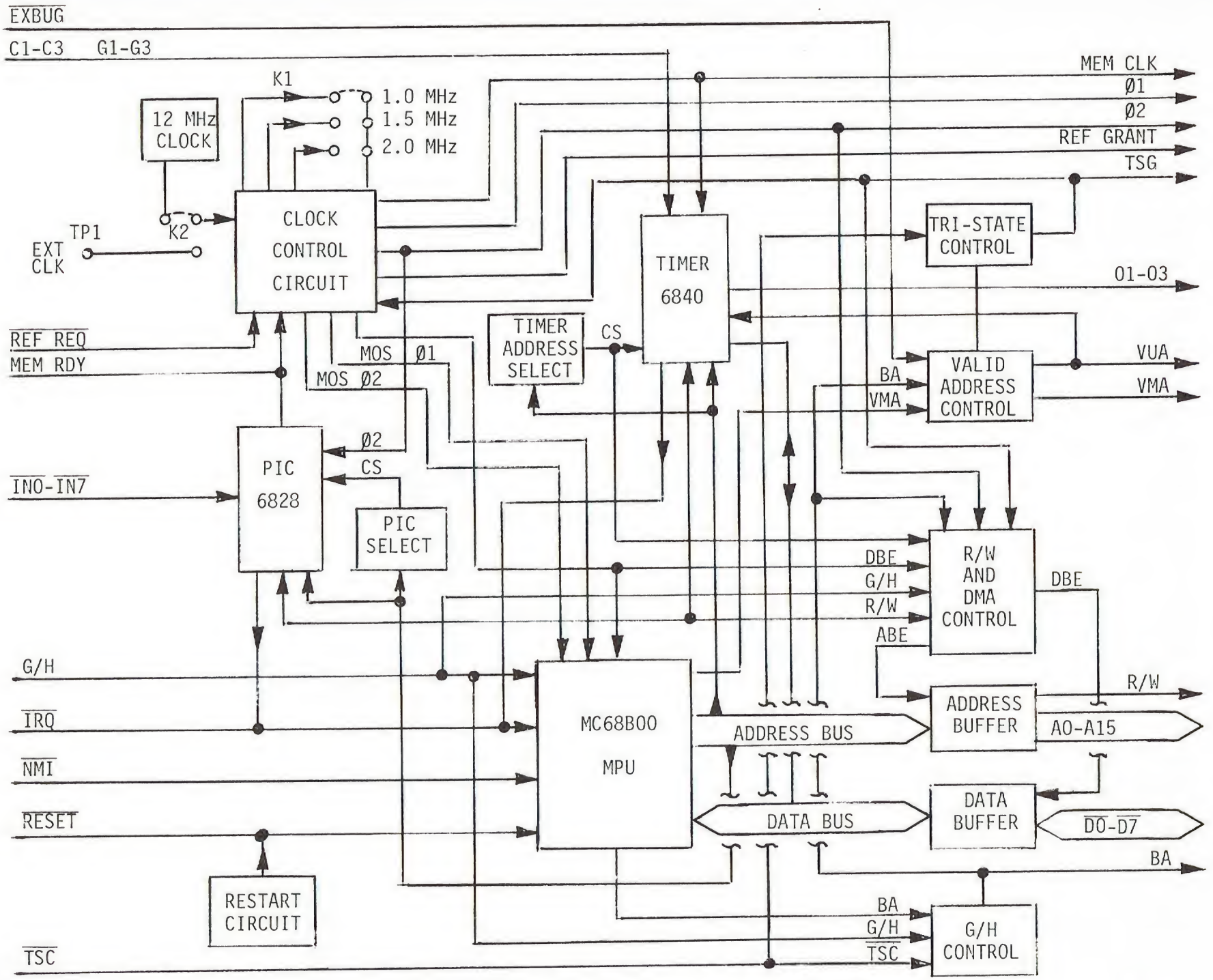


FIGURE 3-1. MPU II Module, Block Diagram

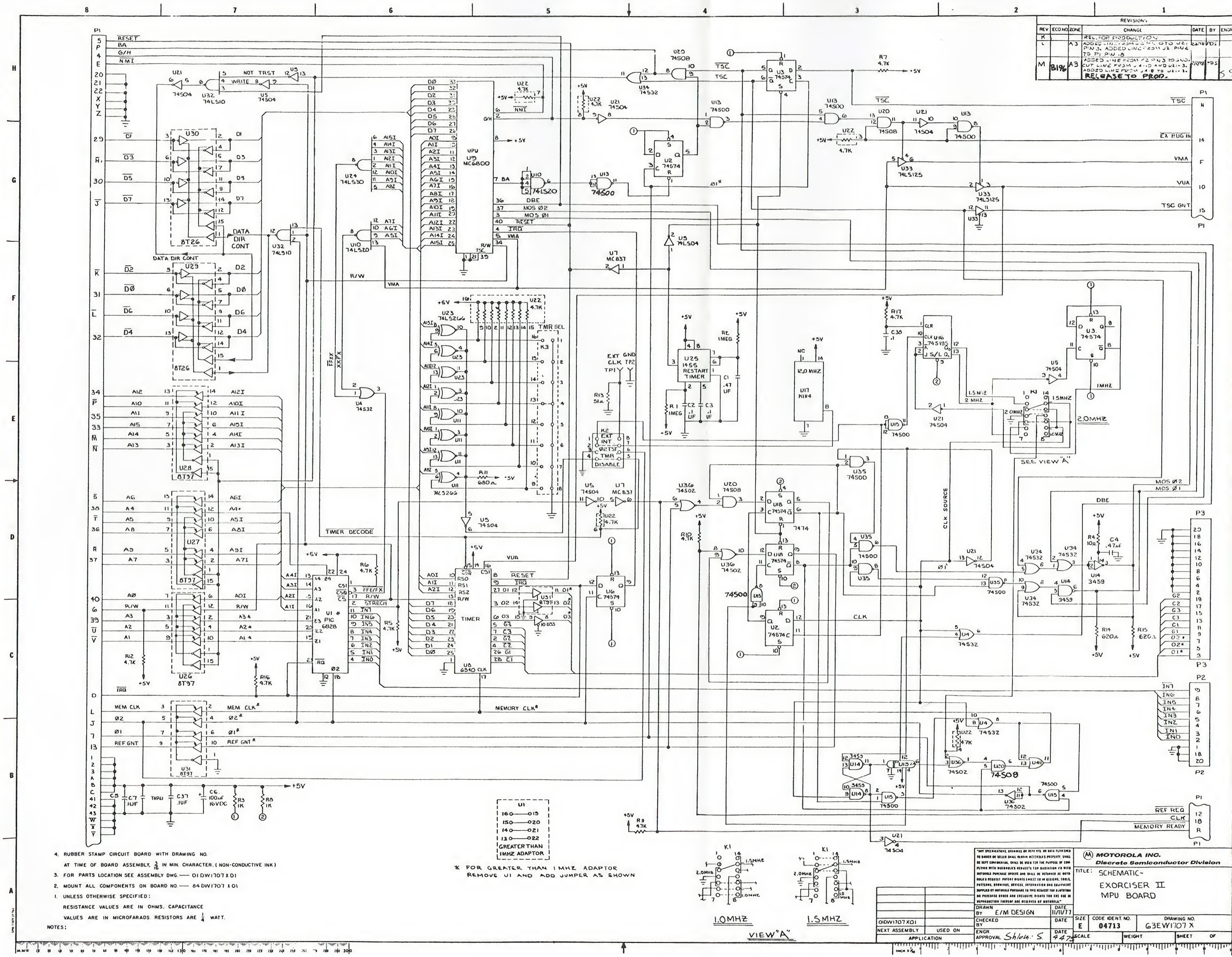


FIGURE 3-2. MPU II Module, Schematic Diagram

CHAPTER 4

PARTS

4.1 INTRODUCTION

This chapter provides the parts list and parts location for the MPU II Module (Table 4-1 and Figure 4-1). The parts list reflects the latest issue of the hardware at the time of printing.

TABLE 4-1. MPU Module Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION	EFFEC-TIVITY
	84DW6707X01	Printed Wiring Board, MPU Module	K
	55NW9403A10	Ejector, Circuit Card, with Roll Pin Attachment, 2 required	K
C1,C4	21NW9604A31	Capacitor, Fixed, Ceramic, 0.47 MFD @ 100 VDC	K
C2,C3,C5,C7-C19, C21-C38	21NW9702A09	Capacitor, Fixed, Ceramic 0.1 MFD @ 50 VDC	K
C6	23NW9618A09	Capacitor, Electrolytic, 100 MFD @ 16 VDC	K
K1	28NW9802C36	Header, Double Row Post, 14 Pin	K
K2,K3	28NW9802C43	Header, Double Row Post, 8 Pin (Use 2 at K3)	K
P2	28NW9802C12	Header, Double Row Post, 20 Pin	K
R1,R2	06SW-124B22	Resistor, Fixed, Carbon, 1.0 MEG OHM, 5%, 1/4W	K
R3,R8	06SW-124A49	Resistor, Fixed, Carbon 1K OHM, 5%, 1/4W	K
R4	06SW-124A01	Resistor, Fixed, Carbon, 10 OHM, 5%, 1/4W	K
R5,R6,R7,R9,R10, R12,R16,R17	06SW-124A65	Resistor, Fixed, Carbon, 4.7K OHM, 5%, 1/4W	K
R11,R14,R15	06SW-124A45	Resistor, Fixed, Carbon, 680 OHM, 5%, 1/4W	K
R13	06SW-124A18	Resistor, Fixed, Carbon, 51 OHM, 5%, 1/4W	K
TP1,TP2	29NW9805A44	Terminal, Stud, Turret, Sub-Miniature	K
U1	51NW9615D80	I.C. MC6828P	K
U2,U3,U6,U18	51NW9615C95	I.C. SN74S74N	K
U4,U34	51NW9615D27	I.C. SN74S32N	K
U5,U21	51NW9615C96	I.C. SN74S04N	K

TABLE 4-1. MPU Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION	EFFEC-TIVITY
U7	51NW9615F08	I.C. MC837P	K
U8	51NW9615D81	I.C. MC6840P	K
U9	51NW9615F14	I.C. MC68B00	K
U10	51NW9615F05	I.C. SN74S20N	K
U11,U23	51NW9615F09	I.C. SN74S266J	K
U12		Not used	
U13,U15,U35	51NW9615C94	I.C. SN74S00N	K
U14	51NW9615B38	I.C. MC3459L	K
U16	51NW9615F11	I.C. SN74S195N	K
U17	48NW9606A24	Crystal Oscillator, 12 MHz	K
U19	01NW9804B33	Module, Digital Delay, 250 ns	K
U20	51NW9615C56	I.C. SN74S08N	K
U22	51NW9626A13	Resistor Network, 15/4.7K OHM, 16 Pin	K
U24	51NW9615C23	I.C. SN74LS30N	K
U25	51NW9615B65	I.C. MC1455P1	K
U26,U27,U28,U31	51NW9615B71	I.C. 8T97	K
U29,U30	51NW9615F19	I.C. 8T26A	K
U32	51NW9615E88	I.C. 74LS10A	K
U33	51NW9615F10	I.C. SN74LS125J	K
U36	51NW9615D32	I.C. SN74S02N	K
	28NW9802B09	Socket, I.C., 40 Pin (use at U9)	K
	28NW9802B08	Socket, I.C., 24 Pin (use at U1)	K
	28NW9802B93	Socket, I.C., 28 Pin (use at U8)	K
	01BW1659X01	Header, 24 Pin (use at U1)	K
	29NW9805A91	Jumper, 2 position (3 for K2, 2 for K2, 1 for K3)	K

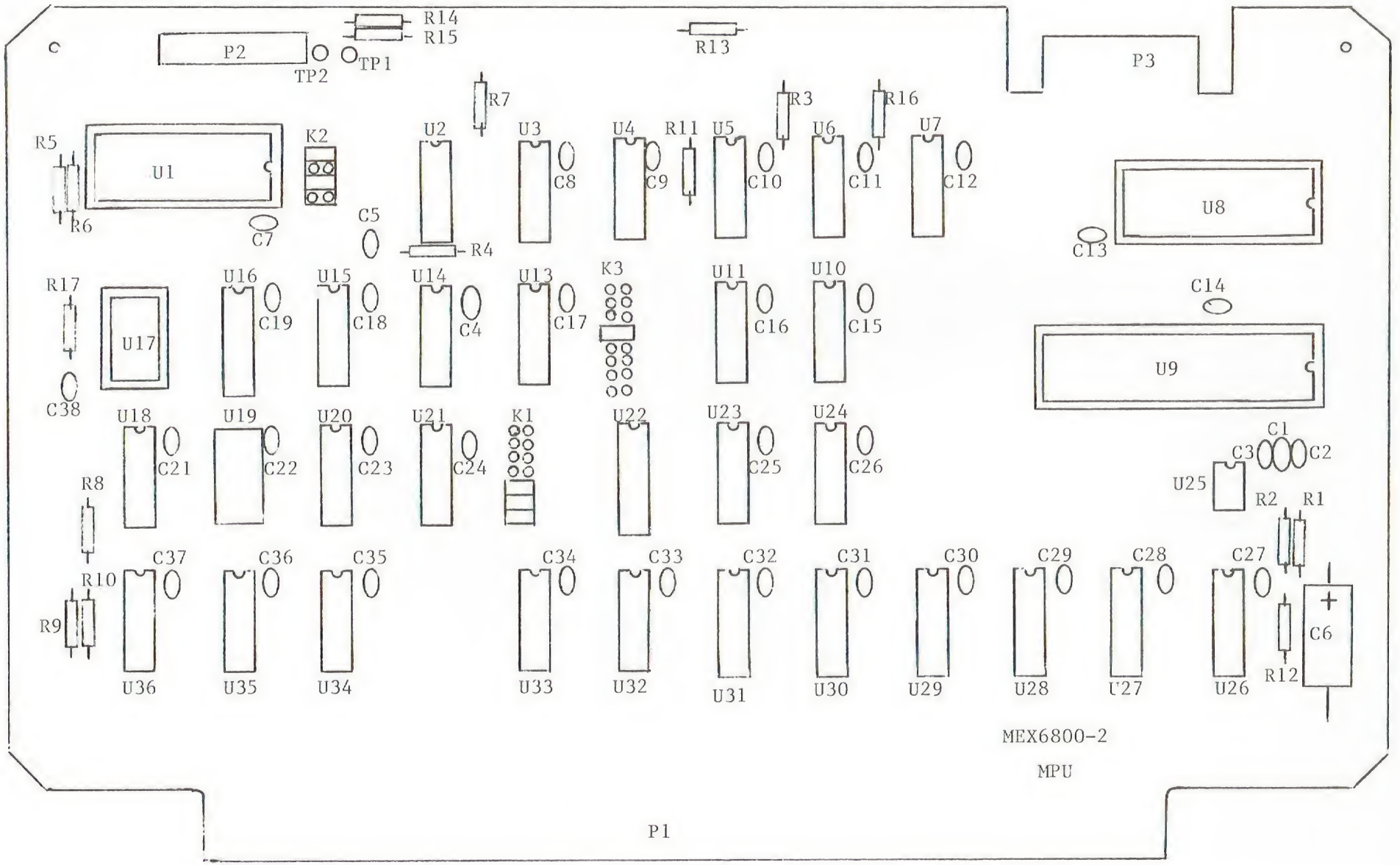


FIGURE 4-1. MPU II Module, Parts Location